

# United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,329	12/04/2003	Daoqiang Lu	P16918	7363
28062 75	90 03/14/2006		EXAM	INER
•	MASCHOFF, TALWAL	AFZALI,	AFZALI, SARANG	
5 ELM STREET NEW CANAAN, CT 06840		ART UNIT	PAPER NUMBER	
	,		3729	· · · · · · · · · · · · · · · · · · ·

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
Office Action Summer	10/728,329	LU ET AL.				
Office Action Summary	Examiner	Art Unit				
	Sarang Afzali	3729				
- The MAILING DATE of this communication appears on the cover sheet with the correspondence address - Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on <u>Amendment filed 2/14/2006</u> .						
a) ☐ This action is <b>FINAL</b> . 2b) ☑ This action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-12,16-18 and 23</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-12,16-18 and 23</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or	election requirement.					
Application Papers						
9) The specification is objected to by the Examiner.						
10) ☐ The drawing(s) filed on is/are: a) ☐ acce	epted or b) objected to by the E	Examiner.				
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>						
Attachment(s)  1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)						
<ol> <li>Notice of References Cited (PTO-892)</li> <li>Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date</li> </ol>	Paper No(s)/Mail Da					

#### **DETAILED ACTION**

### Response to Amendment

1. The applicant's amendment filed on 2/14/2006 has been fully considered and made of record.

## Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 3. Claims 1-12, 16-18, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Stratas (US 5,722,159).

As applied to claim 1, Stratas teaches a method of assembling a semiconductor package wherein a chuck (120, Fig. 15) picking up a clip (12, Fig. 15) and while chuck (120) is holding the clip (12), it picks up the IC die (14 and 80, Fig. 17) wherein the IC die (14 and 80) is in direct contact with the clip (12, Fig. 17).

As applied to claim 2, Stratas teaches a method wherein a vacuum chuck (120) is used to pick up IC die (Fig. 17).

As applied to claim 3, Stratas teaches a method wherein the vacuum is applied to the IC die (14 and 80) via an aperture in the clip. Note that the picking up of the die is facilitated via the use of the aperture (24) in the clip (12) to readily identify the correct IC die prior to be picked up by vacuum chuck (120, col. 5, lines 17-21).

Application/Control Number: 10/728,329

Art Unit: 3729

As applied to claim 4, Stratas teaches a method wherein the IC die (14 and 80) is in contact with a polymer pad that is part of the clip (12, Fig. 17). Note that clip (12) is preferably formed from injection molded plastic, which is polymer (col. 5, lines 4-5).

As applied to claims 5-7, and 23, Stratas teaches a method wherein the chuck (120) is used to simultaneously place the clip (12) and IC die (14 and 80) into juxtaposition with a heat spreader and further releases the clip and the IC die from the chuck while holding the IC die in place on the heat spreader with the clip and bonding the IC die to the heat spreader while holding the IC die in place on the heat spreader with the clip (Figs. 20a-20b). Note that printed circuit board (16, Fig. 20b) is a heat spreader and/or an adhesive layer between the back of IC die (14) and printed circuit board (16) serves as a heat spreader (col. 11, lines 8-16).

As applied to claim 8, Stratas teaches a method wherein the clip (12) may be removed (if needed) from the IC die (14 and 80) and from the heat spreader (printed circuit board 16, col. 5, lines 47-53) after soldering of the IC die (14).

As applied to claims 9 and 10, Stratas teaches a method wherein before bonding (solder reflow, col. 11, lines 8-10) the IC die (14 and 80) to the heat spreader (printed circuit board 16, Fig. 20b), chuck (120) releases (Fig. 20b) the clip (12) and the IC die (14 and 80) and then transporting (through oven, col. 11, line 9) the heat spreader (printed circuit board 16) with the IC die held in place on the heat spreader by the clip (12, Fig. 20b).

As applied to claim 11, Stratas teaches a method wherein the bonding includes reflowing a solder layer on the heat spreader (col. 11, lines 8-10).

Application/Control Number: 10/728,329

Art Unit: 3729

As applied to claim 12, Stratas teaches a method wherein the chuck 9120) simultaneously places the clip (12) and the IC die (14 and 80) into juxtaposition with a package substrate (printed circuit board 16, Fig. 20b).

As applied to claim 16, Stratas teaches a method of assembling a semiconductor package comprising:

holding a clip (12, Fig. 15) in a chuck a chuck (120, Fig. 15) such that an aperture in the clip is aligned with an aperture in the chuck;

picking up an integrated circuit (IC) die (14 and conductive trace 80, Fig. 17) by applying a vacuum to the die via the apertures in the clip (aperture 24 in clip 12, Figs. 2 & 16) and in the chuck (Fig. 16); Using the chuck to simultaneously place the clip and the IC die into juxtaposition with a heat spreader (printed circuit board 16, Fig. 20b);

releasing the clip and the IC die from the chuck while holding the IC die in place on the heat spreader with the clip (Fig. 20b); and

Soldering the IC die (14) to the heat spreader while holding the IC die in place on the heat spreader with the clip (Fig. 20b).

Note that the aperture in the middle of chuck (120) is aligned with the aperture in the middle of the clip (12, Fig. 16).

Note that the picking up of the die is done such that the aperture (24) in the clip (12) is used to readily identify the correct IC die to be picked up and the aperture in the chuck (col. 8, lines 57-62) is used to grip the clip.

Art Unit: 3729

Note that printed circuit board (16, Fig. 20b) is a heat spreader and/or an adhesive layer between the back of IC die (14) and printed circuit board (16) serves as a heat spreader (col. 11, lines 8-16).

As applied to claim 17, Stratas teaches a method wherein the clip (12) may be removed (if needed) from the IC die (14 and 80) and from the heat spreader (printed circuit board 16, col. 5, lines 47-53) after soldering of the IC die (14).

As applied to claim 18, Stratas teaches a method wherein the IC die (14 with 80) is held by the chuck (120) with the clip (12) interposed between the IC die and the chuck (Fig. 20b).

### Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Note that Chan (US 6,629,363) and Spigarelli et al. (US 5,317,803) use chuck and clip by means of vacuum to pick up IC die for assembling on heat spreader and package substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarang Afzali whose telephone number is 571-272-8412. The examiner can normally be reached on 7:00-3:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 10/728,329

Art Unit: 3729

Page 6

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S.A.

03/08/2006

George Nguyen/-Primary Examiner